Q.E.D.* Emulators For the Intel386™ Processor Family

- Up to 33 MHz Target Operation
- Licensed Intel Bondout Technology Combined with Patented Emulator Technology
- 10 Mbits Per Second Communication Channel
- Plug-In and Run Operation, Fully Supports Intel's ONCE* Mode and All Package Configurations
- Two Source Level Debug Interfaces Support All Memory Models
- Hardware Execution Breakpoints Limited Only by Overlay RAM
- Hardware Event System Has Two Modes for Hardware Debug and Software Debug
- 16K (64K Optional) Trace Memory Fully Qualified by Hardware Event System
- 1024K Overlay Memory Standard

Q.E.D.*-386Ex is a small full feature emulator for your Intel386™ processor project. The entire product fits in your pocket! We combine Intel's technology with our own high density ASIC technology to insure true transparent and exact emulator functionality.

Q.E.D.-386Ex integrates into your existing development environment. We offer support for all popular compilers as well as tight integration with the leading operating system products. Q.E.D.-386Ex has a robust and flexible, state machine driven bus event system and a wide and deep trace memory buffer to deliver next generation capability to the user. No matter whether your code runs real mode or protected segmented mode, Q.E.D. offers a development solution best matched to your environment.

The Hardware Bus Event System has two modes to optimize its internal architecture to either Hardware or Software debug requirements. The bus events can combine into one large group of many execution events ("Flat Mode") or it combines into two groups of execution events ("Logic Analyzer Mode"). Each event combines

comparitors for ADDR with DATA and STATUS. In addition, each event independently accesses 16 channels of Logic State Input channels and 16-bit hardware event pass counter. The number of execution breakpoints is limited only by the amount of Overlay RAM in the emulator system.

The 64K trace buffer captures all ADDR, DATA, STATUS information, along with a 16-bit timestamp and up to 16 channels of Logic State Inputs (LSI). The trace display shows any combination of source, assembly and raw cycles interleaved for true execution history clarity, and the trace can be fully qualified by the Bus Event System for PRE, POST, and MIDDLE triggers. The timestamp uses 5 timebases – 100 nsec to 1 msec – that are independent of the target CLK; counter overflow is captured automatically to insure accurate long duration measurements. A special timestamp mode measures the MIN, MAX and MEAN interval time statistic.

Overlay RAM is 0-wait state at 33 MHz operation and it may be mapped across the entire target address space on 1K boundaries. Each segment can be access protected.

Finally with Q.E.D. Emulators, you can fine tune the development tool capabilities to your team's individual requirements.

HOST SYSTEMS SUPPORTED:
486 PC or above (386 PC minimum), 4 MB RAM, Microsoft Windows* or OS2 Warp or MS-DOS 6.0 or above, ISA, MCA or PCMCIA version II, type II expansion card slot.

PROCESSORS SUPPORTED:
Intel386 EX processor - 33 MHz @ 5V,
Intel386 EX processor - 20 MHz @ 3V

AVAILABILITY:
Now

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